19-2326; Rev 0; 1/02

MAXIM

Differential LVPECL-to-LVDS Translators

General Description

The MAX9374 and MAX9374A are 2.0GHz differential LVPECL-to-LVDS translators and are designed for telecom applications. They feature 250ps propagation delay. The differential output conforms to the ANSI TIA/EIA-644 LVDS standard. The inputs are biased with internal resistors such that the output is differential low when inputs are open. An on-chip V_{BB} reference output is available for single-ended operation.

The MAX9374 is designed for low-voltage operation from a 2.375V to 2.625V power supply for use in 2.5V systems. The MAX9374A is designed for 3.0V to 3.6V operation in systems with a nominal 3.3V supply. Both devices are offered in industry-standard 8-pin SOT23 and SO packages.

Features

- **Guaranteed 2.0GHz Operating Frequency**
- **250ps (typ) Propagation Delay**
- **1.0ps RMS Jitter (typ)**
- **2.375V to 2.625V Low-Voltage Supply Range (MAX9374)**
- **On-Chip V_{BB} Reference for Single-Ended Input**
- **Output Low for Open Inputs**
- **Output Conforms to ANSI TIA/EIA-644 LVDS Standard**
- **ESD Protection >2.0kV (Human Body Model)**
- **Available in Small 8-Pin SOT23 Package**

Applications

Precision Clock Buffer

Low-Jitter Data Repeater

Central Office Clock Distribution

DSLAM/DLC

Base Station

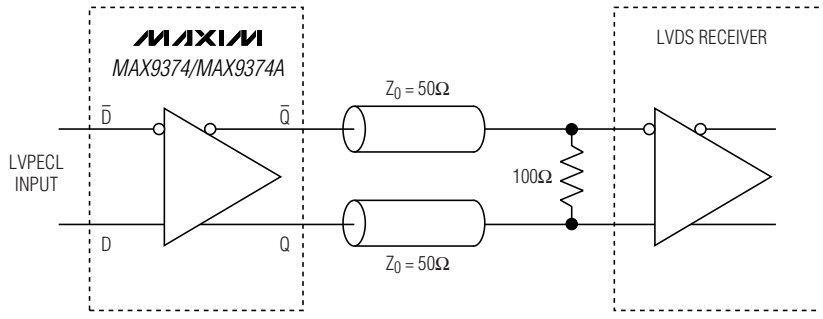
Mass Storage

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX9374EKA-T	-40°C to +85°C	8 SOT23-8	AAKU
MAX9374ESA	-40°C to +85°C	8 SO	—
MAX9374AEKA-T	-40°C to +85°C	8 SOT23-8	AAKV
MAX9374AESA	-40°C to +85°C	8 SO	—

Pin Configurations/Functional Diagrams appear at end of data sheet.

Typical Application Circuit



Differential LVPECL-to-LVDS Translators

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND 4.0V
V_D, $V_{\overline{D}}$ to GND .....-0.3V to V_{CC} + 0.3V
V_D to $V_{\overline{D}}$ 3.0V
V_{BB} Sink/Source Current 1mA
Short-Circuit Duration (Q, $\overline{Q}$ to GND) .....Continuous
Short-Circuit Duration (Q to $\overline{Q}$) .....Continuous
Continuous Power Dissipation (T_A = +70°C)
8-Pin SOT23 (derate 8.9mW/°C above +70°C) 714mW
8-Pin SO (derate 5.9mW/°C above +70°C) 470mW
Junction-to-Ambient Thermal Resistance
8-Pin SOT23 .....+112°C/W
8-Pin SO .....+170°C/W
Junction-to-Ambient Thermal Resistance with 500 LFPM Airflow
8-Pin SOT23 .....+78°C/W
8-Pin SO .....+99°C/W
Junction-to-Case Thermal Resistance
8-Pin SOT23 .....+80°C/W
8-Pin SO .....+40°C/W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
ESD Protection
Human Body Model (D, $\overline{D}$, Q, $\overline{Q}$) 2kV
Soldering Temperature (10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.375V to 2.625V for MAX9374, V_{CC} = 3.0V to 3.6V for MAX9374A, 100Ω ±1% across outputs, V_{ID} = 0.095V to V_{CC} or 3V, whichever is less, V_{IHD} = 1.2V to V_{CC}, V_{ILD} = GND to V_{CC} - 0.095V, unless otherwise noted. Typical values are at V_{IHD} = 2.0V, V_{ILD} = 1.85V, V_{CC} = 3.3V for MAX9374A, V_{CC} = 2.5V for MAX9374.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DIFFERENTIAL INPUT (D, $\overline{D}$)												
High Voltage of Differential Input	V_{IHD}	Figure 1	1.2		V_{CC}	1.2		V_{CC}	1.2		V_{CC}	V
Low Voltage of Differential Input	V_{ILD}	Figure 1	GND		V_{CC} - 0.095	GND		V_{CC} - 0.095	GND		V_{CC} - 0.095	V
Single-Ended Input High Voltage	V_{IH}	V_{BB} connected to $\overline{D}$ (V_{IL} for V_{BB} connected to D), Figure 1	V_{CC} - 1.165		V_{CC}	V_{CC} - 1.165		V_{CC}	V_{CC} - 1.165		V_{CC}	V
Single-Ended Input Low Voltage	V_{IL}	V_{BB} connected to $\overline{D}$ (V_{IH} for V_{BB} connected to D), Figure 1	V_{EE}		V_{CC} - 1.475	V_{EE}		V_{CC} - 1.475	V_{EE}		V_{CC} - 1.475	V
Differential Input Voltage	V_{IHD} - V_{ILD}	V_{CC} < 3.0V	0.1		V_{CC}	0.1		V_{CC}	0.1		V_{CC}	V
		V_{CC} ≥ 3.0V	0.1		3.0	0.1		3.0	0.1		3.0	
Input Current	I_{IN}	V_{IHMAX}, V_{ILMIN} (Note 3)	-150		150	-150		150	-150		150	µA
DIFFERENTIAL OUTPUT (Q, $\overline{Q}$)												
Output High Voltage	V_{OH}	Figure 1			1.6			1.6			1.6	V
Output Low Voltage	V_{OL}	Figure 1	0.9			0.9			0.9			V
Differential Output Voltage	V_{OD}	Figure 1	250	350	450	250	350	450	250	350	450	mV

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.375V to 2.625V for MAX9374, V_{CC} = 3.0V to 3.6V for MAX9374A, 100Ω ±1% across outputs, V_{ID} = 0.095V to V_{CC} or 3V, whichever is less, V_{IHD} = 1.2V to V_{CC}, V_{ILD} = GND to V_{CC} - 0.095V, unless otherwise noted. Typical values are at V_{IHD} = 2.0V, V_{ILD} = 1.85V, V_{CC} = 3.3V for MAX9374A, V_{CC} = 2.5V for MAX9374.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Change in V_{OD} Between Complementary Output States	ΔV_{OD}			1	25		1	25		1	25	mV
Output Offset Voltage	V_{OS}		1.125	1.25	1.375	1.125	1.25	1.375	1.125	1.25	1.375	V
Change in V_{OS} Between Complementary Output States	ΔV_{OS}			3	25		3	25		3	25	mV
Output Short-Circuit Current	I_{OSC}	Q or $\overline{Q}$ short to GND		23	30		23	30		23	30	mA
V_{BB} AND SUPPLY												
Reference Voltage	V_{BB}	I_{BB} = ±0.6mA (Note 4)	V_{CC} - 1.38		V_{CC} - 1.26	V_{CC} - 1.38		V_{CC} - 1.26	V_{CC} - 1.38		V_{CC} - 1.26	V
Supply Current	I_{CC}	(Note 5)		16	30		18	30		20	30	mA

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.375V to 2.625V for MAX9374, V_{CC} = 3.0V to 3.6V for MAX9374A, 100Ω ±1% across outputs, V_{IHD} - V_{ILD} = 0.15V to V_{CC} or 3V, whichever is less, V_{IHD} = 1.2V to V_{CC}, V_{ILD} = GND to V_{CC} - 0.15V, f_{IN} = 1GHz, input transition time = 125ps, input duty cycle = 50%, unless otherwise noted. Typical values are at V_{IHD} = 2.0V, V_{ILD} = 1.85V, V_{CC} = 3.3V for MAX9374A, V_{CC} = 2.5V for MAX9374, unless otherwise noted.) (Notes 1, 6)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Differential Input to Differential Output Delay	t_{PLHD}, t_{PHLD}	Figure 1	116	240	420	128	250	403	145	260	440	ps
Single-Ended Input to Differential Output Delay	t_{PLHS}, t_{PHLS}	Figure 1	126	250	430	138	250	415	155	260	450	ps
Part-to-Part Skew	t_{SKPP}	(Note 7)			304			275			295	ps
Added Random Jitter (Note 8)	t_{RJ}	f_{IN} = 1.0GHz, clock pattern		0.9	2		1	2		1	2	$ps_{(RMS)}$
		f_{IN} = 2.0GHz, clock pattern		0.8	2		0.9	2		0.9	2	
Added Deterministic Jitter (Note 8)	t_{DJ}	f_{IN} = 2.0Gbps, 2^{23} -1 PRBS pattern		45	75		46	75		38	75	$ps_{(P-P)}$
Operating Frequency	f_{MAX}	V_{OD} ≥ 250mV	2.0	2.2		2.0	2.2		2.0	2.2		MHz
Output Rise/Fall Time	t_R, t_F	20% to 80%, Figure 1		92	200		91	200		90	200	ps

AC ELECTRICAL CHARACTERISTICS (continued)

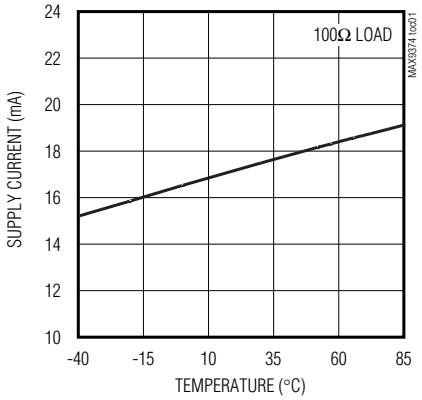
(V_{CC} = 2.375V to 2.625V for MAX9374, V_{CC} = 3.0V to 3.6V for MAX9374A, 100Ω ±1% across outputs, V_{IHD} - V_{ILD} = 0.15V to V_{CC} or 3V, whichever is less, V_{IHD} = 1.2V to V_{CC}, V_{ILD} = GND to V_{CC} - 0.15V, f_{IN} = 1GHz, input transition time = 125ps, input duty cycle = 50%, unless otherwise noted. Typical values are at V_{IHD} = 2.0V, V_{ILD} = 1.85V, V_{CC} = 3.3V for MAX9374A, V_{CC} = 2.5V for MAX9374, unless otherwise noted.) (Notes 1, 6)

Note 1: Measurements are made with the device in thermal equilibrium.
Note 2: DC parameters are production tested at T_A = +25°C and guaranteed by design over the full operating temperature range.
Note 3: Current into a pin is defined as positive. Current out of a pin is defined as negative.
Note 4: Use V_{BB} as a reference for inputs on the same device only.
Note 5: 100Ω across the outputs, all other pins open except V_{CC} and GND.
Note 6: Guaranteed by design and characterization. Limits are set at ±6 sigma.
Note 7: Measured between outputs of different parts at the signal crossing points under identical conditions for a same-edge transition.
Note 8: Device jitter added to the input signal.

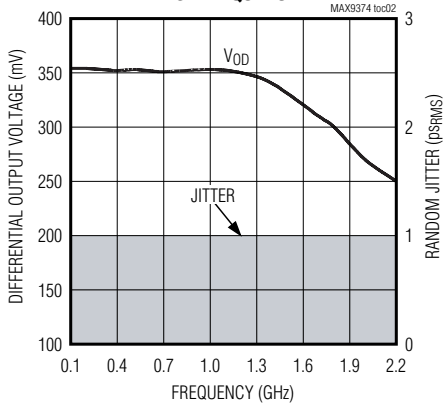
Typical Operating Characteristics

(MAX9374A, 100Ω ±1% across outputs, f_{IN} = 1GHz, input transition time = 125ps, input duty cycle = 50%, V_{CC} = 3.3V, V_{IHD} = 2.0V, V_{ILD} = 1.85V, T_A = +25°C, unless otherwise noted.)

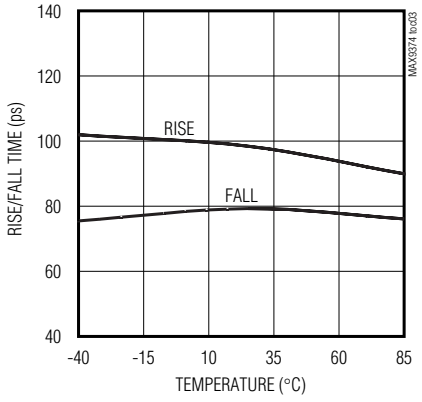
SUPPLY CURRENT vs. TEMPERATURE



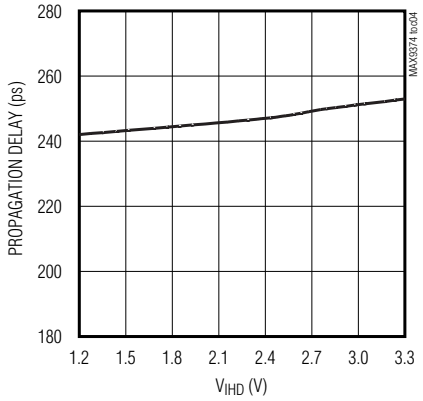
DIFFERENTIAL OUTPUT VOLTAGE (V_{OD}) vs. FREQUENCY



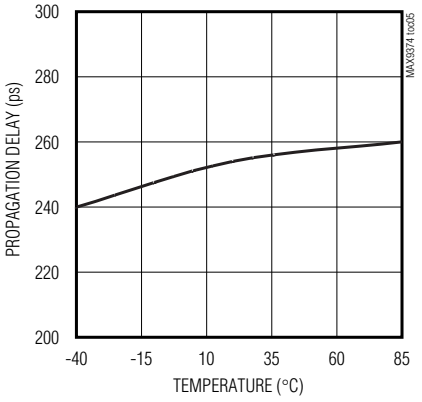
RISE/FALL TIME vs. TEMPERATURE



PROPAGATION DELAY vs. HIGH VOLTAGE OF DIFFERENTIAL INPUT (V_{IHD})



PROPAGATION DELAY vs. TEMPERATURE



Pin Description

PIN		NAME	FUNCTION
SOT23	SO		
1	4	V_{BB}	Reference Output Voltage. Connect to the inverting or noninverting data input to provide a reference for single-ended operation. When used, bypass with a 0.01µF ceramic capacitor to V_{CC}; otherwise, leave it open.
2	5	GND	Ground. Provide a low-impedance connection to the ground plane.
3	3	$\overline{D}$	Inverted LVPECL Data Input. 36.5kΩ pullup to V_{CC} and 75kΩ pulldown to GND.
4	2	D	Noninverted LVPECL Data Input. 75kΩ pullup to V_{CC} and 75kΩ pulldown to GND.
5	8	V_{CC}	Positive Supply Voltage. Bypass V_{CC} to GND with 0.1µF and 0.01µF ceramic capacitors. Place the capacitors as close to the device as possible with the smaller value capacitor closest to the device.
6	7	Q	Noninverted LVDS Output. Typically terminate with 100Ω to $\overline{Q}$.
7	6	$\overline{Q}$	Inverted LVDS Output. Typically terminate with 100Ω to Q.
8	1	N.C.	No Connection. Not internally connected.

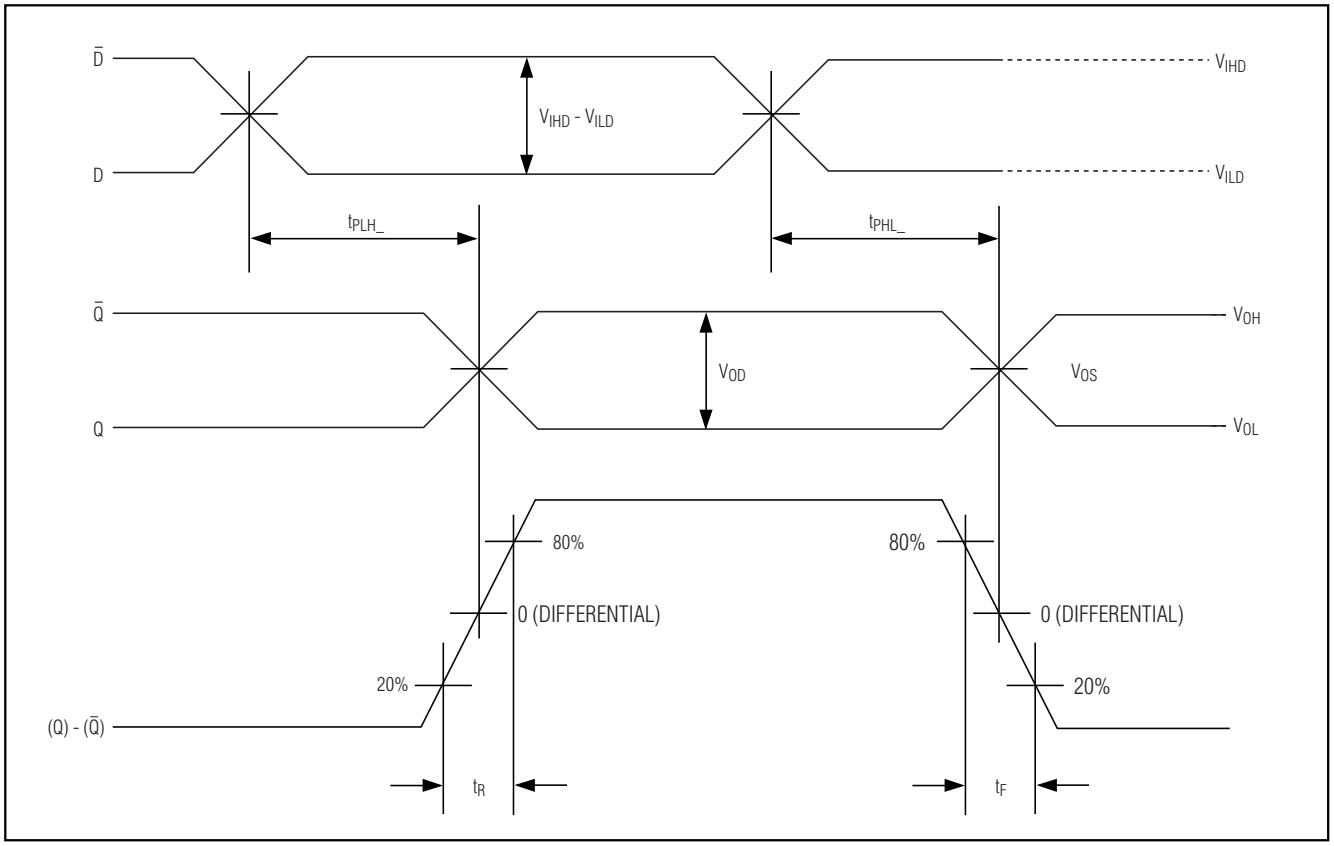


Figure 1. MAX9374/MAX9374A Timing Diagram

Differential LVPECL-to-LVDS Translators

Detailed Description

The MAX9374/MAX9374A are 2.0GHz differential LVPECL-to-LVDS translators. The output is differential LVDS and conforms to the ANSI TIA/EIA-644 LVDS standard. The inputs are biased with internal resistors such that the output is differential low when inputs are open. An on-chip V_{BB} reference output is available for single-ended input operation. The MAX9374 is designed for low-voltage operation from 2.375V to 2.625V in systems with a nominal 2.5V supply. The MAX9374A is designed for 3.0V to 3.6V operation in systems with a nominal 3.3V supply.

Differential LVPECL Input

The MAX9374/MAX9374A accept differential LVPECL inputs and can be configured to accept single-ended inputs through the use of the V_{BB} voltage reference output. The maximum magnitude of the differential signal applied to the input is 3.0V or V_{CC}, whichever is less. This limit also applies to the difference between any reference voltage input and a single-ended input. Specifications for the high and low voltages of a differential input (V_{IHD} and V_{ILD}) and the differential input voltage (V_{IHD} - V_{ILD}) apply simultaneously.

Single-Ended Inputs and V_{BB}

The differential inputs can be configured to accept a single-ended input through the use of the V_{BB} reference voltage. A noninverting, single-ended input is produced by connecting V_{BB} to the $\overline{D}$ input and applying a single-ended input signal to the D input. Similarly, an inverting input is produced by connecting V_{BB} to the D input and applying the input signal to the $\overline{D}$ input. With a differential input configured as single ended (using V_{BB}), the single-ended input can be driven to V_{CC} and GND or with a single-ended LVPECL signal. Note that a single-ended input must be at least V_{BB} ±95mV or a differential input of at least 95mV to switch the outputs to the V_{OH} and V_{OL} levels specified in the *DC Electrical Characteristics* table.

When using the V_{BB} reference output, bypass it with a 0.01µF ceramic capacitor to V_{CC}. If the V_{BB} reference is not used, leave it unconnected. Use V_{BB} only for inputs that are on the same device as the V_{BB} reference.

Input Bias Resistors

Internal biasing resistors ensure a (differential) output-low condition in the event that the inputs are not connected. The inverting input ($\overline{D}$) is biased with a 36.5kΩ pulldown to V_{CC} and a 75kΩ pullup to GND. The noninverting input (D) is biased with a 75kΩ pullup to V_{CC} and 75kΩ pulldown to GND.

Differential LVDS Output

The differential outputs conform to the ANSI TIA/EIA-644 LVDS standard. Typically, terminate the outputs with 100Ω across Q and $\overline{Q}$, as shown in the *Typical Application Circuit*. The outputs are short-circuit protected.

Applications Information

Supply Bypassing

Bypass V_{CC} to GND with high-frequency surface-mount ceramic 0.1µF and 0.01µF capacitors in parallel and as close to the device as possible, with the 0.01µF capacitor closest to the device. Use multiple parallel vias to minimize parasitic inductance. When using the V_{BB} reference output, bypass it with a 0.01µF ceramic capacitor to V_{CC} (if the V_{BB} reference is not used, it can be left open).

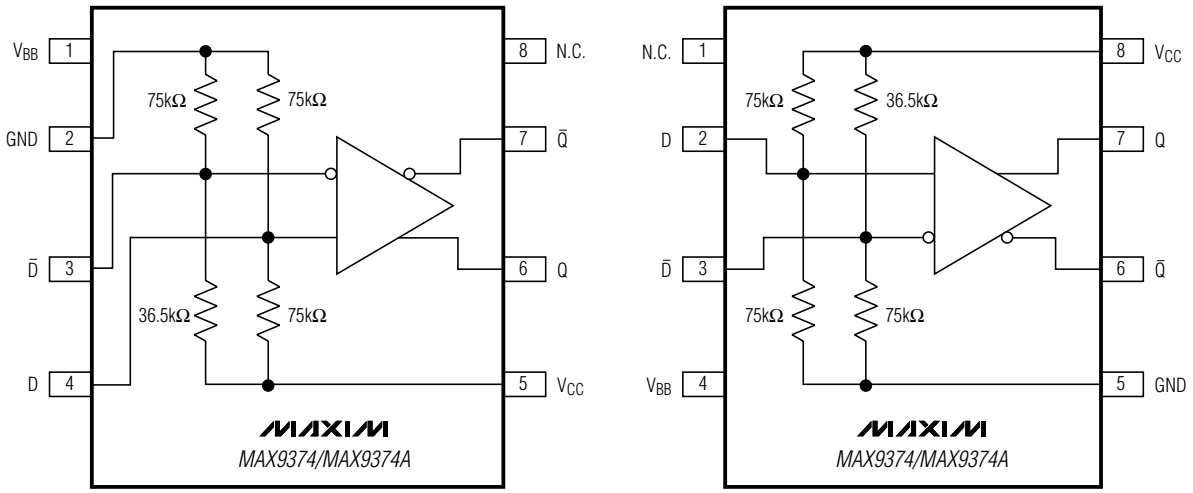
Controlled-Impedance Traces

Input and output trace characteristics affect the performance of the MAX9374/MAX9374A. Connect high-frequency input and output signals to 50Ω characteristic impedance traces. Minimize the number of vias to prevent impedance discontinuities. Reduce reflections by maintaining the 50Ω characteristic impedance through cables and connectors. Reduce skew within a differential pair by matching the electrical length of the traces.

Output Termination

Terminate the outputs with 100Ω across Q and $\overline{Q}$ as shown in the *Typical Application Circuit*. Both outputs must be terminated.

Pin Configurations/Functional Diagrams



SOT23 **SO**

Chip Information

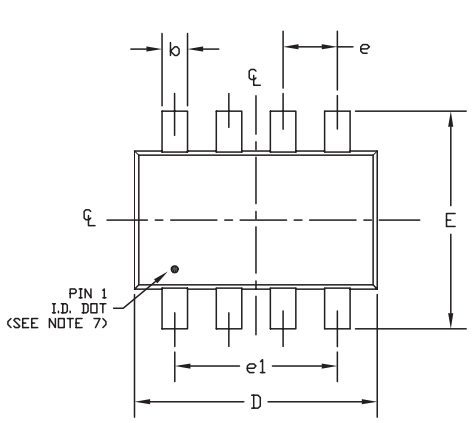
TRANSISTOR COUNT: 236

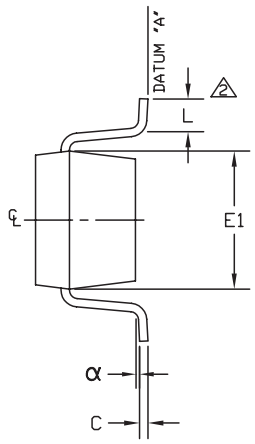
PROCESS: Bipolar

Differential LVPECL-to-LVDS Translators

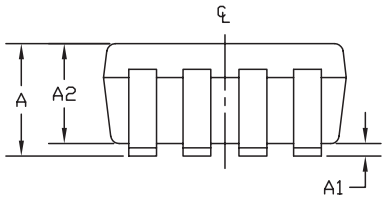
Package Information

SOT23, 8L.EPS





SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.28	0.45
C	0.09	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.10	0.60
e	0.65 ref	
e1	1.95 ref	
α	0°	10°



NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED REFERENCE TO FLAT FOOT SURFACE PARALLEL TO DATUM "A".
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. EIAJ REF. NUMBER" SC-74 (6 LEAD VERSION)
6. COPLANARITY 4 MILS. MAX.
7. PIN 1 I.D. DOT IS 0.3 MM ø MIN. LOCATED ABOVE PIN 1.
8. MEETS JEDEC MO178.

MAXIM

PROPRIETARY INFORMATION

TITLE:

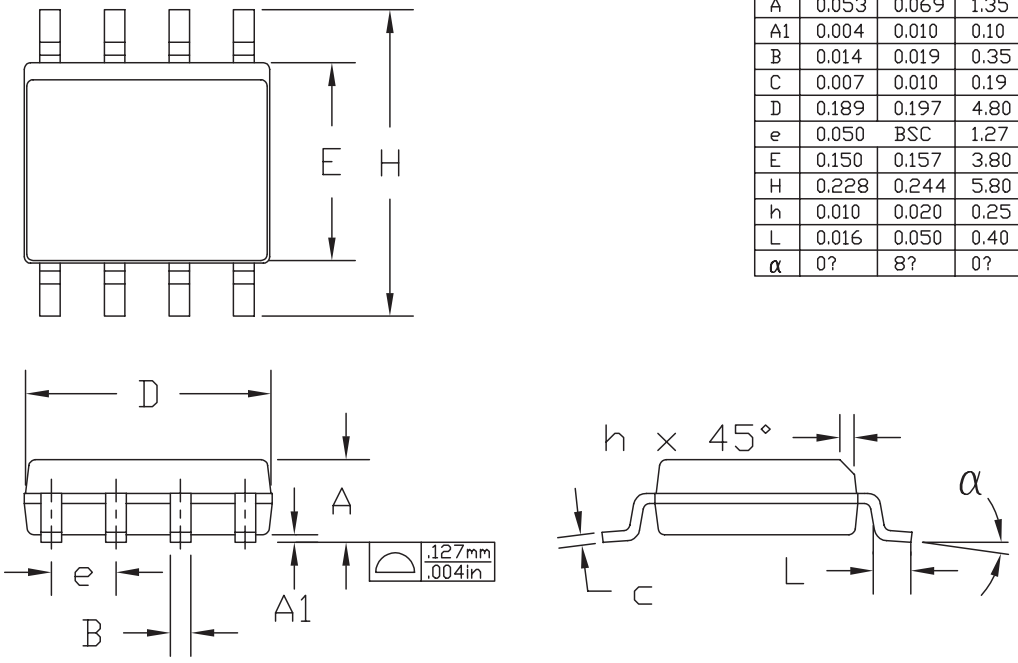
PACKAGE OUTLINE, SOT-23, 8L

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0078	C	1/1

Package Information (continued)

9LUCSP, 3x3.EPS

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
D	0.189	0.197	4.80	5.00
e	0.050	BSC	1.27	BSC
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27
α	0?	8?	0?	8?



NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS-012 AA.

MAXIM
PROPRIETARY INFORMATION

TITLE: 8L SOIC OUTLINE

APPROVAL	DWG	REV	
	21-0325	A	1/1